The system should look like the following block diagram. It has a FIFO with 12bits with and 16 elements, and two BRAM (A and B) which are used in ping pong scheme. The BRAMs are same with 48bits width and 1024 depth.

The input data at FIFO write side, should be random 12 bits data that are generated randomly as well, i.e. some clocks there are new data and some other clocks there are not. It should generate new data in 66% of the times. For that, for every clock cycle a random integer number can be generated in the range of 0~2, if the value is zero, it should not generate a new data, and if it 1 or 2, then it should generate the next data. The write side of the FIFO should work with 400MHz and the read side with 100MHz. In one period of data generation, 4096 data should be generated, and after a time gap, the next period will be started.

The data are stored in a packed way (4 data in one memory row i.e., 4 \* 12bits = 48bits) in memory A and B. The memories are selected in a ping-pong way. Once a memory is filled completely, the next memory is selected to store the next data set, and in between the filled memory data is read out and compared with the generated data to check the correctness of the whole process.

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FIFO, Width: 12bits, Depth: 16

Mem-A

Width: 48bits

Depth: 1024

Mem-B

Width: 48bits

Depth: 1024

Data Equality checking

Random 12-bits Data Generator